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1. A delay circuit comprising:

a plurality of current mirror current sources, with each current mirror current source having an enable input, having an input for receiving an input signal and having a constant current output for providing a constant current responsive to the input signal;

a plurality of current mirror current drains, with each current mirror current drain having an enable input, having an input for receiving the input signal, and having a constant drain output for providing a constant current responsive to the input signal;

a programmable delay control circuit having a plurality of enable signals, each signal connected to a current mirror current source and current mirror current drain such that the programmable delay control circuit selectively enables a pair of current mirror current source and drain;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current outputs of the plurality of current mirror current sources and to the constant drain outputs of the plurality of current drains, the second plate connected to a voltage reference, with each current mirror current source having a current path between a corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor and with, each current mirror current drain having a current path between the corresponding enable signal of said programmable delay control circuit and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output responsive to the voltage on the capacitor;

wherein a delay on the rising edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current sources to

change an overall current source current provided by the plurality of current mirror current sources to the first plate of the capacitor, and

wherein a delay on the falling edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current drains to change an overall current drain current provided by the plurality of current mirror current drains to the first plate of the capacitor.

2. The delay circuit of claim 1 wherein the programmable delay control circuit comprises a digital circuit.

3. The delay circuit of claim 2 wherein the digital circuit comprises programmable memory circuit.

4. The delay circuit of claim 3 wherein the programmable memory circuit comprises a programmable read only memory.

5. The delay circuit of claim 4 wherein the programmable read only memory comprises a EEPROM.

6. The delay circuit of claim 3 wherein the programmable memory circuit comprises a FLASH memory.

7. A delay circuit comprising:

a first input transistor having a control element for receiving an input signal, and having a current path with a first end connected to a voltage source and a second end;

a second input transistor having a control element for receiving the input signal, and having a current path with a first end and a second end connected to a voltage reference;

a first bias transistor having a current path with a first end connected to the voltage source, having second end, and having a control element, wherein the second end is connected to the control element and to the second end of the current path of the first input transistor;

a resistor having a first end connected to the second end of said first bias transistor and having a second end;

a second bias transistor having a current path from the second end of said resistor to the voltage reference, and having a control element connected to the second end of said resistor and to the first end of the current path of said second input transistor;

a capacitor having a first plate and having a second plate connected to the voltage reference;

an output stage having an input connected to the first plate of said capacitor and having an output;

a programmable delay control circuit having a plurality of enable outputs;

a plurality of constant-current sources, each constant current source of the plurality of constant-current sources having a current path between a corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said first bias transistor such that the current flowing in the first bias transistor is proportionately mirrored in the current path of each constant-current source of the plurality of constant-current sources, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current source; and

a plurality of constant-current drains, each constant current drain of the plurality of constant-current drains having a current path between the corresponding enable output of said programmable delay control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said second bias transistor such that the current flowing in the second bias transistor is proportionately mirrored in the current path of each constant-current drain of the plurality of constant-current drains, responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current drain.

8. The delay circuit of claim 7 wherein said programmable delay control circuit comprises a digital circuit.

9. The delay circuit of claim 8 wherein the digital circuit comprises programmable memory circuit.

10. The delay circuit of claim 9 wherein the programmable memory circuit comprises a programmable read only memory.

11. The delay circuit of claim 10 wherein the programmable read only memory comprises a EEPROM.

12. The delay circuit of claim 9 wherein the programmable memory circuit comprises a FLASH memory.

13. A delay circuit comprising:

a plurality of current mirror current elements, with each current mirror current element having an enable input, having an input for receiving an input signal and having a constant current output for providing a constant current responsive to the input signal;

a programmable delay control circuit having a plurality of enable signals, each enable signal connected to the plurality of current mirror current elements so as to selectively enable a current mirror current element of the plurality of current mirror current elements;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current outputs of the plurality of current mirror current elements, the second plate connected to a voltage reference, with each current mirror current element having a current path between a corresponding enable signal of said programmable delay and control circuit and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output responsive to the voltage on the capacitor; [,]

wherein a delay on an active edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current elements to change an overall current provided by the plurality of current mirror current elements to the first plate of the capacitor.

14. The delay circuit of claim 13, wherein the active edge of the input signal is a rising edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current sources, and a delay on the rising edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current sources to change an overall current source current provided by the plurality of current mirror current sources to the first plate of the capacitor.

15. The delay circuit of claim 13, wherein the active edge of the input signal is a falling edge of the input signal and the plurality of current mirror current elements are a plurality of current mirror current drains, and a delay on the falling edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the enable signal of one or more of the plurality of current mirror current drains to change an overall current drain current provided by the plurality of current mirror current drains to the first plate of the capacitor.

16. A delay circuit comprising:

a current-mirror current source having an enable input, an input for receiving an input signal, and a constant-current output for providing a constant current responsive to the input signal;

a current-mirror current drain having an enable input, an input for receiving the input signal, and a constant drain output for providing a constant current responsive to the input signal;

a programmable delay-control circuit operable to generate an enable signal on an enable output that is coupled to the current-mirror current source and the current-mirror current drain such that the programmable delay-control circuit selectively enables the current-mirror current source and the current-mirror current drain;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant current output of the current-mirror current source and to the constant drain output of the current drain, the second plate connected to a voltage reference, the current-mirror current source having a current path between the enable output and the first plate of said capacitor and the current-mirror current drain having a current path between the enable output and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output signal responsive to the voltage on the capacitor;

wherein a delay on the rising edge of the input signal is adjustable by the programmable delay-control circuit selectively enabling the enable signal to change an overall current source current provided to the first plate of the capacitor, and

wherein a delay on the falling edge of the input signal is adjustable by the programmable delay-control circuit selectively enabling the enable signal to change an overall current drain current provided to the first plate of the capacitor.

17. A delay circuit comprising:

a first input transistor having a control element for receiving an input signal, and having a current path with a first end connected to a voltage source and a second end;

a second input transistor having a control element for receiving the input signal, and having a current path with a first end and a second end connected to a voltage reference;

a first bias transistor having a current path with a first end connected to the voltage source, having second end, and having a control element, wherein the second end is connected to the control element and to the second end of the current path of the first input transistor;

a resistor having a first end connected to the second end of said first bias transistor and having a second end;

a second bias transistor having a current path from the second end of said resistor to the voltage reference, and having a control element connected to the second end of said resistor and to the first end of the current path of said second input transistor;

a capacitor having a first plate and having a second plate connected to the voltage reference;

an output stage having an input connected to the first plate of said capacitor and having an output;

a programmable delay-control circuit having one or more enable outputs;

one or more constant-current sources each having a source current path between a corresponding enable output of said programmable delay-control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said first bias transistor such that the current flowing in the first bias transistor is proportionately mirrored in the source current path responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current source; and

one or more constant-current drains each having a drain current path between a corresponding enable output of said programmable delay-control circuit and the first plate of said capacitor, and having a bias input connected to the control element of said second bias transistor such that the current flowing in the second bias transistor is proportionately mirrored in the drain current path responsive to the corresponding enable output and wherein a constant of proportionality may be chosen independently of the constant of proportionality of any other constant-current drain.

18. A delay circuit comprising:

one or more current-mirror current elements each having an enable input, an input for receiving an input signal, and a constant-current output for providing a constant current responsive to the input signal;

a programmable delay control circuit operable to generate one or more enable signals, each enable signal connected to a respective one of the one or more current-mirror current elements so as to selectively enable the respective current-mirror current element;

a fixed capacitor having a first plate and a second plate, the first plate of the capacitor connected to the constant-current outputs of the one or more current-mirror current elements, the second plate connected to a voltage reference, each current-mirror current element having a current path between a respective one of the one or more enable signals and the first plate of said capacitor; and

an output stage having an input connected to the first plate of the capacitor and having an output for providing an output signal responsive to the voltage on the capacitor;

wherein a delay on an active edge of the input signal is adjustable by the programmable delay control circuit selectively enabling the one or more enable signals to change an overall current provided by the one or more current-mirror current elements to the first plate of the capacitor.

19. A delay circuit, comprising:

a energy-storage element;

a current circuit coupled to the energy-storage element and operable to receive an input signal having first and second levels, to source a first constant current to the energy-storage element in response to the input signal having the first level, and to sink a second constant current from the energy-storage element in response to the input signal having the second level; and

an output circuit coupled to the energy-storage element and operable to generate a delayed signal.

20. The delay circuit of claim 19 wherein the energy-storage element comprises a capacitor.

21. The delay circuit of claim 19, further comprising:

a control circuit coupled to the current circuit and operable to generate an enable signal; and

wherein the current circuit comprises a current stage operable to source a third constant current to the energy-storage element in response to the enable signal and in response to the input signal having the first level, and operable to sink a fourth constant current from the energy-storage element in response to the enable signal and in response to the input signal having the second level.

22. The delay circuit of claim 19, further comprising:

a control circuit coupled to the current circuit and operable to generate an enable signal; and

wherein the current circuit comprises a current stage operable to source a third constant current to the energy-storage element in response to the enable signal and in response to the input signal having the first level, and operable to sink a fourth constant current from the energy-storage element in response to the enable signal and in response to the input signal having the second level, the third and fourth constant currents less than or equal to the first and second constant currents, respectively.

23. The delay circuit of claim 19, further comprising:

a control circuit coupled to the current circuit and operable to generate enable signals; and

wherein the current circuit comprises current stages each operable to source a respective third constant current to the energy-storage element in response to a respective one of the enable signals and in response to the input signal having the first level, and operable to sink a respective fourth constant current from the energy-storage element in response to the respective one of the enable signals and in response to the input signal having the second level.

24. The delay circuit of claim 19, further comprising:

a control circuit coupled to the current circuit and operable to generate enable signals; and

wherein the current circuit comprises current stages each operable to source a respective third constant current to the energy-storage element in response to a respective one of the enable signals and in response to the input signal having the first level, and operable to sink a respective fourth constant current from the energy-storage element in response to the respective one of the enable signals and in response to the input signal having the second level, a sum of the respective third constant currents being less than or equal to the first constant current and a sum of the respective fourth constant currents being less than or equal to the second constant current.

25. The delay circuit of claim 19 wherein the first constant current equals the second constant current.

26. The delay circuit of claim 19 wherein the first and second levels respectively comprise a logic high and a logic low level.

27. The delay circuit of claim 19 wherein the output circuit comprises an inverter having an output node and having an input node coupled to the energy-storage element, the inverter operable to generate the delayed signal on the output node.

28. The delay circuit of claim 19 wherein the output circuit comprises:

a first inverter having an output node and having an input node coupled to the energy-storage element; and

a second inverter having an output node and having an input node coupled to the output node of the first inverter, the second inverter operable to generate the delayed signal on the output node of the second inverter.

29. A delay circuit, comprising:

a energy-storage element;

a control circuit operable to generate enable signals;

a current circuit coupled to the energy-storage element and to the control circuit and operable to receive an input signal having first and second levels, the current circuit including current stages that are each operable to source a respective first constant current to the energy-storage element in response to the input signal having the first level and in response to a respective one of the enable signals and operable to sink a respective second constant current from the energy-storage element in response to the input signal having the second level and in response to the respective one of the enable signals; and

an output circuit coupled to the energy-storage element and operable to generate a delayed signal.

30. The delay circuit of claim 29 wherein the current circuit comprises:

a current generator operable to generate a third constant current in response to the input signal having the first level and to generate a fourth constant current in response to the input signal having the second level; and

wherein each current stage is operable to mirror the third constant current in response to the input signal having the first level and to mirror the fourth constant current in response to the input signal having the second level.

31. The delay circuit of claim 29 wherein the current circuit comprises:

a current generator operable to generate a third constant current; and

wherein each current stage is operable to mirror the third constant current.

32. A method, comprising:

delaying a first edge of an input signal by charging an energy-storage element with a first constant current in response to the input signal transitioning from a first level to a second level; and

delaying a second edge of the input signal by discharging the energy-storage element with a second constant current in response to the input signal transitioning from the second level to the first level.

33. The method of claim 32 wherein the first constant current equals the second constant current.

34. The method of claim 32, further comprising:

wherein the energy-storage element comprises a capacitor;

generating a delayed signal having a third level when a voltage across the capacitor is less than a predetermined level; and

generating the delayed signal having a fourth level when the voltage across the capacitor is greater than the predetermined level.

35. The method of claim 32, further comprising:

wherein the energy-storage element comprises a capacitor;

generating a delayed signal having the first level when a voltage across the capacitor is less than a predetermined level; and

generating the delayed signal having the second level when the voltage across the capacitor is greater than the predetermined level.